NR

Code No: A0601, A5701

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, March/April 2011

DIGITAL SYSTEM DESIGN

(COMMON TO DIGITAL SYSTEMS AND COMPUTER ELECTRONICS, VLSI STSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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1.a) Draw the state diagram, state table and ASM chart for a D Flip-Flop.

b) Discuss the different components of ASM chart. [12]

2.a) Implement the logic function 'F' using ROM

$F = \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C + ABC$

b) Explain how a sequential circuit can be designed using CPLD? [12]

3.a) Show that the three paths indicated in the circuit as shown in Fig. 1 cannot be sensitized individually but can be sensitized simultaneously.

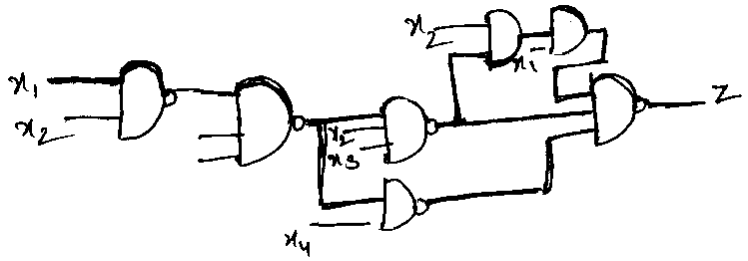

Fig:1

b) Classify faults and give some examples to each class. [12]

4.a) Write a D Algorithm and compare it with other test pattern generation methods.

b) How signature analysis is used for testing bridging faults? [12]

5. Consider the machine whose transition table is given in table shown in Fig 2. Design a checking experiment for this machine. [12]

q \ x	a	b	c	d
A	A, 0	B, 1	A, 0	D, 1
B	C, 1	A, 0	B, 0	A, 0
C	D, 1	B, 1	A, 1	B, 0
D	B, 0	C, 1	A, 1	C, 1

Fig: 2

Contd…2

6.a) What is PLA folding? Why it is needed?

b) Implement the following three Boolean functions with a PLA.

$F_1(A, B, C) = \varepsilon(0, 1, 2, 4)$

$F_2(A, B, C) = \varepsilon(0, 5, 6, 7)$

$F_3(A, B, C) = \varepsilon(0, 3, 5, 7)$ [12]

7. Explain how to test a PLA circuits? [12]

8.a) Draw & Explain the Basic model of sequential circuit.

b) Give a state assignment without critical races to each of the following asynchronous machine shown in figure 3. [12]

q \ x	I_0	I_1	I_2	I_3
A	(A)	C	(A)	B
B	A	(B)	A	(B)
C	(C)	(C)	E	D
D	C	B	(D)	(D)
E	(E)	F	(E)	D
F	E	(F)	A	B

Fig: 3

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